CLAIMS

1. (Previously Presented) A drive circuit for delivering high-level power to a load, the drive circuit comprising:

a high power circuit including a set of semiconductor switching devices capable of being coupled to the load and delivering the high level power thereto; a logic circuit generating signals to control the semiconductor switching devices;

a low power circuit to transmit the signal from the logic circuit to the high power circuit; only when the low power circuit is receiving electrical power; and

a safety circuit electrically independent of the logic circuit to control the application of power to the low power circuit.

2. (Cancelled)

3. (Previously Presented) The drive circuit of claim 1, wherein the safety circuit is a safety relay that is coupled to a power terminal of the low power circuit, and wherein the safety relay decouples the power terminal of the low power circuit from a power supply in order to disable the low power circuit.

4. (Previously Presented) The drive circuit of claim 1, wherein the safety circuit is a safety relay that is coupled to a pull-up resistor of the low power circuit, and wherein the safety relay disables the low power circuit by at least one of coupling the pull-up resistor to ground and decoupling the pull-up resistor from a power supply.

5. (Withdrawn) The drive circuit of claim 4, wherein the safety relay additionally is coupled to a power terminal of the low power circuit, and wherein the safety relay couples the power terminal of the low power circuit to ground in order to further disable the low power circuit.

6. (Previously Presented) The drive circuit of claim 4, wherein the safety relay includes a coil, a normally-open contact, and a normally-closed contact, wherein

the contacts are physically coupled so that only one of the contacts can be closed at any given time, and wherein the safety relay disables the low power circuit when power is provided to the coil.

7. (Previously Presented) The drive circuit of claim 1, wherein the safety circuit is coupled to an override port of the low power circuit, and wherein the safety circuit disables the low power circuit by providing a first signal to the override port of the low power circuit.

8. (Previously Presented) The drive circuit of claim 7, wherein the safety circuit includes a hardware switch that is capable of being switched between first and second states, and wherein, when the switch is switched in the first state, the safety circuit provides the first signal to the override port of the low power circuit.

9. (Previously Presented) The drive circuit of claim 8, wherein the safety circuit further includes a NOR gate having first and second input terminals, wherein the NOR gate receives a second signal from the hardware switch and a third signal from the low power circuit at the first and second input terminals, and wherein the NOR gate outputs a fourth signal that is one of equal to or functionally related to the first signal.

10. (Original) The drive circuit of claim 8, wherein the high power circuit includes at least one coil that outputs a signal indicative of a current delivered by the high power circuit to the load, and wherein a determination is made regarding whether the signal indicative of the current is proper when the switch is switched in the first state.

11. (Previously Presented) The drive circuit of claim 1, wherein the low power circuit includes an inverter circuit, and a buffer circuit.

12. (Previously Presented) The drive circuit of claim 11 wherein, when the low power circuit is not disabled, the logic circuit outputs a plurality of preliminary

signals to the inverter circuit, the inverter circuit converts the plurality of preliminary signals into a plurality of modified signals, and the buffer circuit provides the at least one control signal in response to the plurality of modified signals, and each of the preliminary signals, the modified signals, and the at least one control signal is a pulse width modulated (PWM) signal.

13. (Previously Presented) The drive circuit of claim 11, wherein the inverter circuit has open collector output terminals that are coupled to the buffer circuit, wherein the safety circuit is a safety relay that is coupled to a pull-up resistor that is coupled between the safety relay and both one of the open collector output terminals and a corresponding input terminal of the buffer circuit, and wherein the safety relay at least one of decouples the pull-up resistor from a power supply and couples the pull-up resistor to a ground in order to disable the low power circuit.

14. (Previously Presented) The drive circuit of claim 13, wherein the safety relay also is coupled to an additional pull-up resistor that is coupled to a third circuit portion that is coupled to an enable input of the buffer circuit, and wherein the safety relay at least one of decouples the additional pull-up resistor from the power supply and couples the additional pull-up resistor to the ground in order to further disable the low power circuit by disabling the buffer circuit.

15. (Previously Presented) The drive circuit of claim 1, wherein the high power circuit includes a plurality of high power transistor devices that are light-actuated and a plurality of photodiodes receive the at least one control signal from the lower power circuit, and wherein the high power transistor devices are electrically isolated from the photodiodes.

16. (Withdrawn) The drive circuit of claim 1, wherein the safety circuit is an isolation device that is capable of communicating a signal provided from an additional device to the low power circuit.

17. (Withdrawn) The drive circuit of claim 16, wherein the isolation device includes one of a DC-to-DC converter and an optical isolator.

18-23. (Cancelled)

24. (Previously Presented) A motor drive circuit for delivering high-level power to a load, the drive circuit comprising:

a high power circuit including a set of semiconductor switching devices capable of being coupled to the load and delivering the high level power thereto; a logic circuit generating signals to control the semiconductor switching devices;

a low power circuit to transmit the signal from the logic circuit to the high power circuit; only when the low power circuit is receiving electrical power; and

a set of ports exposed by the drive allowing connection of a safety circuit electrically independent of the logic circuit to the drive to control the application of power to the low power circuit.